SCREEN PRINTABLE POLYMERS FOR WAFER LEVEL PACKAGING: A TECHNOLOGY ASSESSMENT

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ABSTRACT

Screen print patterning is an attractive alternative to traditional semiconductor photo-lithography. Our work compared the pattern resolution and mechanical resistance of screen-printed polymers versus spin-on methods. Optical microscopy of screen-printed coatings reveal sharp edge features as well as masked off saw streets and I/Os across the wafer. Thickness comparisons are made between the 2 methodologies. Design rules for screen fabrication, including mesh-count, wire diameter, and emulsion thickness, are discussed. Print parameter recommendations are given for several case studies. Cost models reveal that screen-printing is not just a PCB or substrate level process, but highly suited for wafer handling. Finally, applications of wafer level screen-printing are dissected. It has been shown to be an effective manufacturing process for applying protective coatings for memory die, buffer coatings for wafer thinning technologies, 3D stacked die, bio-MEMs devices, CSP, and optoelectronic packaging.

Key Words: screen print, wafers, MEMs, passivation

INTRODUCTION

Screen and stencil printing technology has been used for many years for printed circuit board (PCB) manufacturing and surface mount component assembly of PCBs. The green-colored solder mask, white component outlines and numbering found on many low-cost PCBs is an epoxy material applied using a screen printing process. Before surface-mount components are placed on a circuit board, solder paste is typically applied over the copper pads using a stencil printing technique.

These processes are similar to ancient silk-screening techniques used for imaging patterns directly onto textile and paper products. Modern screens consist of an interwoven mesh of thin stainless steel wire that supports a photo-imaged emulsion layer. Openings within the emulsion layer enable various inks and epoxy pastes to be squeezed through and transferred onto a flat surface to replicate the pattern imaged within the emulsion layer. Stencil printing is quite similar in concept, except that the wire mesh is replaced with a thin metal or polymer foil through which a pattern of apertures have been cut, plated or etched.

Wafer fabrication has long been dominated by concern for particulate control in order to achieve the minimum feature sizes necessary for state-of-art integrated circuits (ICs). The relatively course geometry limitations for both screen and stencil printing technology has, consequently, been relegated to "back-end" packaging of integrated circuits, or PCB level connections. However, the previously clear distinction between front and back-end wafer processing is becoming blurred due of the need to perform more "packaging" functions while the chips are in wafer-form. [1] With today's increasing need to reduce component size and processing costs, screen and stencil-print technology is finding new application alongside "front-end" wafer fabrication. An example of this is stencil-printed solder paste on whole wafers for flip chip interconnections. And more recently, wafer-level screen-printed coatings are being developed for the protection of bare die.

Non-vacuum based wafer coatings are typically applied by a spin-on technique using the same equipment designed for photo resist patterning. These coatings are typically solvent-based and produce very thin layers. Screen-printed inks and epoxies, on the other hand, are patterned directly onto the wafer's surface and do not require subsequent steps to mask, expose and develop a patterned layer. Since these materials are formulated for screen/stencil print processing, they are typically solvent-free and contain higher solids content than spin-on materials. Hence, these coatings tend to be thicker and more scratch-resistant to provide better protection of minimally packaged ICs. Some advantages of both screen-printed and spin-on coating techniques are summarized below.

Screen-Print Advantages:
1. Fewer and faster process steps (direct patterning without need of a masking, exposure or developing process steps)
2. Less material waste, easier disposal of waste
3. Greater thickness
4. Higher solids content without noxious solvents

5. Less costly equipment and materials
6. No immersion required

Spin-Coat Advantages:
1. Greater dimensional control (photoimagable) for fine geometries
2. Better thinness uniformity
3. Better process control for obtaining very thin coatings
4. Uses same process equipment as used for front-end wafer-fab
5. Non-contact process

Screen printing silver epoxies for surface mount applications is well documented. [2,3,4] At the PCB level, the incentives were high volume area array assembly, due to increased throughput over dispensing methods, while being a drop in replacement for solder paste. Manufacturing with silver epoxy paste, would need to be as simple, proven, and wide-scale as stencil printing solder paste. One group proposed a model for stencil printing process, followed by a factorial design of experiments (DOE) for optimization of the final print patterning. [5]

Due to the momentum decribed above, at the PCB or 2nd level interconnect, we decided to explore the feasability of patterning by screen-printing at the chip, or 1st level interconnect. Although screen-printing cannot begin to match the fine geometries achievable using conventional photoimagable polymers, we feel it is usually sufficient for Chip Scale Packaging (CSP), Flip Chip, and other wafer-level coating requirements. Some examples include protective coating over bio-MEMs devices, alpha particle protection of memory die, passivation isolation of redistributed bond pads, and perimeter edge sealing of glass windows or lids over opto-IC's.

PROCESSING EQUIPMENT USED
The screen printer used for these experimental projects is an MPM-SPM with a custom vacuum platen for holding wafers up to 300mm diameter. A Leitz Secolux 6x6 Microscope and Heidenhain digital counter were used to measure the thickness of the coatings using a difference in focal-height from the substrate to the top-surface of the coatings. Thickness measurements using this method are not as accurate as would be obtained from viewing cross-sections, but are acceptable for the purposes of these evaluations. Typically the epoxy coating thickness would be measured both before and after curing to evaluate the amount of shrinkage that may occur. The wafers were cured in a Lindberg Blue M (model MO1450A) convection-type oven, pre-heated to the proper curing temperature. The epoxy materials were not degassed or stirred by hand prior to printing in order to maintain the proper viscosity and prevent air from becoming

incorporated into the material. The epoxy material would typically be premixed on a three-roll mill or high-shear, counter-rotating, centrifugal mixer, depending on the material being formulated. The centrifugal mixer operates with sufficient speed and shear forces that a considerable amount of air is removed from the mixed epoxy.

DISCUSSION OF RESULTS
Fingerprint Sensors, bio-MEMs
Figure 1 is a photo of a section of a fingerprint sensor with two different screen-printed materials: (a) a clear, UV-cured, orange-peel textured, polymer coating to protect the sensor's cells from scratch and impact damage, and (b) a white border of B-staged epoxy to adhere the sensor chip to a flexible circuit within a cut-out window. Choosing an optimum thickness, one sufficient to ensure protection of the sensor surface without compromising the chip's imaging sensitivity, was derived by printing and curing multiple layers of UV-cured epoxy on individual bare die. One to four layers were printed and cured, measuring in thickness from 9μm to 38μm. Once the ideal thickness was selected (30-32μm), a screen mesh (400 mesh, 0.00075" wire diameter) and emulsion thickness (0.0017") were chosen to coat an entire 200mm wafer using a single print. A similar approach was used to establish an optimal thickness and B-stage cure schedule for the white adhesive border surrounding each sensor chip.
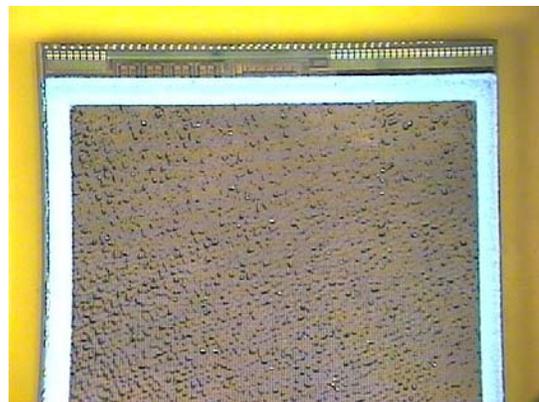
Figure 1. MEMs finger print sensor containing UV cured epoxy coating in the center, with B-stage epoxy resin along the 4 edges.

Another fingerprint chip application required a thin "metallic" colored coating over the surface. A custom formulation, consisting of aluminum flake mixed into a solvent-based resin, achieved the desired color and texture for this particular chip. To assess the printing resolution, the customer designed and submitted a test pattern with graduated and tapered openings. Figure 2 shows a close-up section of test prints made with a single, double and triple layer. Before and after wafer printing, each wafer was weighed to measure how much epoxy

was required for each layer. The average weight for a 25μm thick layer, spread across a 150mm wafer, was 0.25g. After curing (30 minutes at 200°C), each layer shrank to an average thickness of 12-15μm.

Each wafer coating was subjected to mechanical stress testing. Drop tests of 20 cm, and scratch resistance were

Material Used	Pen Scratches	Micro Scratches with Diamond Tip
Standard Spin-On PI, 6μm	Some image degradation with scratches visible; bad columns likely to be generated, PI easily tearded-off	Image degradation with several bad columns and white bands; PI teared-off and passivation scratched
EpoTek K5022-176F 12μm	No image degradation. Higher thickness is likely to contribute; pen causes only compression in the coating. No tear-off observed (material is tougher)	Minor image degradation. Higher thickness os likely to contribute; No tear-off. Material is tougher
EpoTek K5022-176F 5μm	Significant image degradation, starting at 1.0 lbs. At 1.5 lbs. the sensor is non-functional. Performance lower than current polyimide.	Sensors are non-functional. Performance s are lower than standard polymide.

Table I. Mechanical resistance testing of 3 protective coatings over MEMs finger print sensors.

performed. For drop tests, a 1mm diameter medium point, carbide tip, BIC pen, weighing 6 grams, was used. A zero-degree angle, respective to the normal, was used for a no tilt incidence. The number of units consisted of 9 standard spin-on coated wafers, 3 un-coated, and 2 each EPO-TEK coated wafers. The same pen was used for the
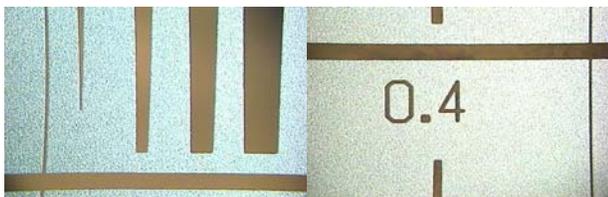
Figure 2. Test Pattern of MEMs finger print sensor having 400 micron mask off area, with tapered and graduated lines for assessing the fine-print resolution.

scratch-testing, consisting of 1-2 lb load, with manual force exerted across 80% of the sensor region. A similar pen was used for the diamond-tip micro-scratch tester,

using 0.2 lb load, at a controlled velocity of 10 mm / min, across a distance of 3mm.
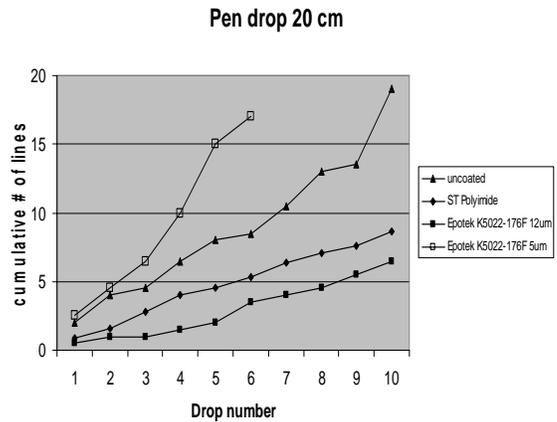
**Figure 3. Drop test results of 3 protective coatings over MEMs finger print sensor.**

The results of the drop test are summarized in Figure 3. Two thicknesses of EPO-TEK screen printable coating were compared against the spin-on polyimide control, and un-coated biometric sensors. The results suggest, as predicted, that a 12 um layer of EPO-TEK coating provided better protection than 5um, and better than a 6um layer of spin-on polyimide. Table 1 provides a final summary of the scratch resistance testing, carbide tip versus diamond. Observations that the 12um screen print coating protected the die better than 5um coating, as well as the spin-on coating, agree well with the drop tests summarized from figure 3.

Alpha Particle Protection of memory die
Memory wafers are prime candidates for chip scale packaging, due to the need of higher integration at a fraction of the PCB real estate. To protect the chip's surface from handling damage and alpha particle induced bit errors, an epoxy-polyimide-based coating was formulated for screen-print patterning. A boron-nitride filler was included as a non-abrasive filler or thixoptropic agent, enabling fine pitch geometry and patterning, as well as to help improve thermal transfer from the die's surface to PCB. Figure 4 shows the pattern for a redistributed ball grid array with 0.009" diameter openings for solder ball placement. The print thickness measured 20-22μm before curing and 14-15μm after curing, which was very close to the 12μm target. Each wafer contained 250 chips, having 128 I/O's per chip. Dimensions were 367 mil x 317 mil, for SRAM die

Only 0.5g of epoxy was required to cover a 200mm wafer using a 400-mesh screen with 0.0002" emulsion. That means about 900 wafers can be screen print coated from 1 lb of polymer passivation. In the competing technology, we have deduced the materials and labor cost associated

with spin-on processes using photo-lithography to be about $35 per wafer, a process that generates more waste than what is used. Our process is completely recyclable, yielding no waste, thus we feel our technology is very compelling, considering the costs benefits.
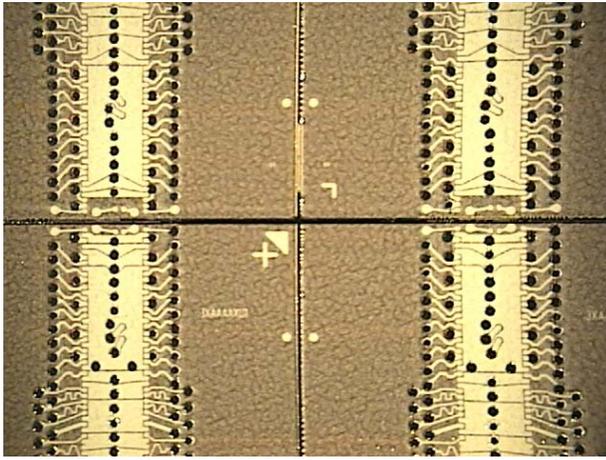
Figure 4. Screen print passivation of redistributed 128 pin BGA-CSP memory device.

Memory Die, Packaging.
A second study involving memory die, in this case DRAM, was investigated. Unlike the application above, which had redistributed bond pads or area array bond pads, this SRAM device used traditonal perimeter lay out around 2 edges only. A sketch of the chip layout is shown in Figure 5. The die size was 248 mil x 146 mil and contained 54 I/O's per chip. The chips were arrayed in a field of 6x3, with 59 fields per 8" wafer, or roughly 1062 chips per wafer. We choose an effective screen print coverage of 227 mil x 146 mil. One half of the 21 mil net difference is the amount of "pull back" of polymer coating per edge. The 10-mil opening was targeted because the bond pad I/O's were 4-mil square, plus an additional 3-mils was added to each side of the pads. In this case, there is no need to print polymer coating up to the edges of each I/O, risking an overcoat of organic residue on the wire bond pads (ref. Figure 6B).
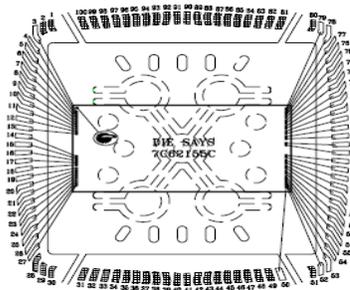

Figure 5. Layout of a 54-pin, SMT style memory device.

Table II below shows the results of the wire bond quality tests. Although wire pull was found to be acceptable, ball shear was 4 grams below spec. The trend of NSOP, or "non stick on pads" may have been observed. The spec of 18 grams was not achieved.

PARAMETER USED		
Time	15 / 12	
Power	50 / 55	
Force	28 / 55	
	Ball shear	**Wirepull**
	14	6.6
	15	4.9
	14	5.5
	14	6.3
	17	6.2
	13	5.5
	13	5.6
	17	7.6
	12	7.4
	11	7.7
Min	**11**	**4.9**
Max	**17**	**7.7**
Ave	**14**	**6.33**
Stdev	**1.94**	**0.98**

Table II. Results of wirebond pull-testing.

We theorize that two things can be improved. First a purge of air or N2 gas during box oven curing may alleviate some of the outgassed hydrocarbons from redepositing onto the surface of the I/O's. Secondly, a "pull-back" of 3 mils might not have been enough to prevent polymer passivation from over coating the strips of wire bond pads. Figures 6A and 6B show an acceptable die that has been wire bonded versus a close-up of one die that had been improperly over-coated, yielding NSOP.
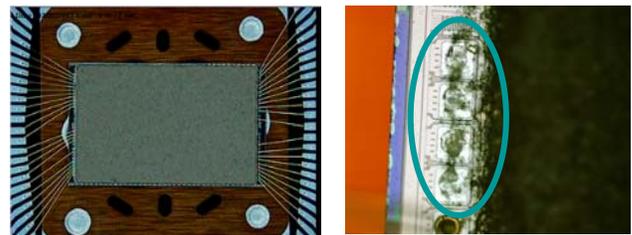

Bonded Units   Encountered NSOP

Figure 6A. Wire bonded memory die showing two mask-off areas on the ends. Figure 6B. Possible source of low wirebond shear strength due to organic bleed-out onto the I/Os.

Opto-Packaging, 625 CSP array
Adhesive sealing around the 4 edges of glass cover slips, is a common packaging method for CSP devices.[6] A glass-Si-glass packaging structure allows for transmission

of visible light range 350 – 900 nm, enabling opto-electronic devices to be realized, such as CMOS and CCD image sensors, found in cell phones and digitial cameras, as well as machine vision applications such as scanners, copiers, and optical pick-up units for DVDs. While some methods of adhesive sealing might use dispensers and capillary forces of medium viscosity resins [7], we find edge sealing to be possible by screen-print methods at the wafer level, instead of single chip glass level.
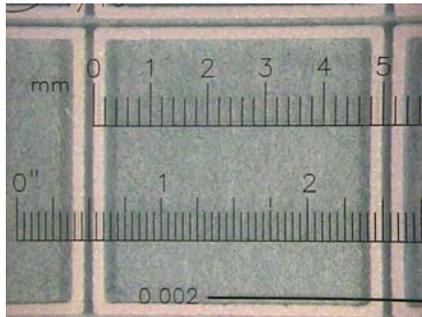

Figure 7. One-up photo of 5mm x 5mm glass die with 4-edge perimeter seal using B-stage epoxy. The chips were arrayed across the wafer in a 25 x 25 format.

We used 8 mil borosilcate glass wafers, which were 14cm x 14cm square, although they could have been received in traditional 8" wafer format. Figure 7 shows the 1 up chip lay-out. 200 um line widths were printed along the 4 edges of the chip. Each chip measured 5mm x 5mm. A 200 um step-and-repeat was used for the X and Y axis saw streets. A total of 625 chips were arrayed in a 25 x 25 format. Final dried print thickness was determined to be 25um for a single print, 40um for double print, and 60um for a triple print. A 325 mesh screen using 1.1 mil wire diameter and 0.4 mil emulstion was used for the project. A solvent containing, B-stageable epoxy was chosen as the adhesive / sealant. This epoxy lends itself to high volume assembly in a down-stream process. Final (A-stage) curing to the second surface can be accomplished using 160 C / 15 seconds + 15N of pressure.

Regarding applications, it is common in the MEMs industry, for glass lids to act as package barrier, or a protective layer above the active chip. [8] Examples are micro-mirror arrays, primarily driven by Texas Instruments and found in fiber optic switching products, and "cap wafers" found in pressure sensors or accelerometers. Figure 8 is a schematic of both devices. With the micro-mirror array, edge sealing of the glass window must be realized, so that IR light from the optical beam pathway is not restricted. In fiber optic switching, laser beams of IR light are re-directed by the on-off pulses of the rotating mirrors. Cap wafers may also be called "structured", or "support wafers", as they "support" the active MEMs chip by acting like a rigid

host carrier, as well as sealing out atmosphere, moisture, and other contaminants that could damage the IC.
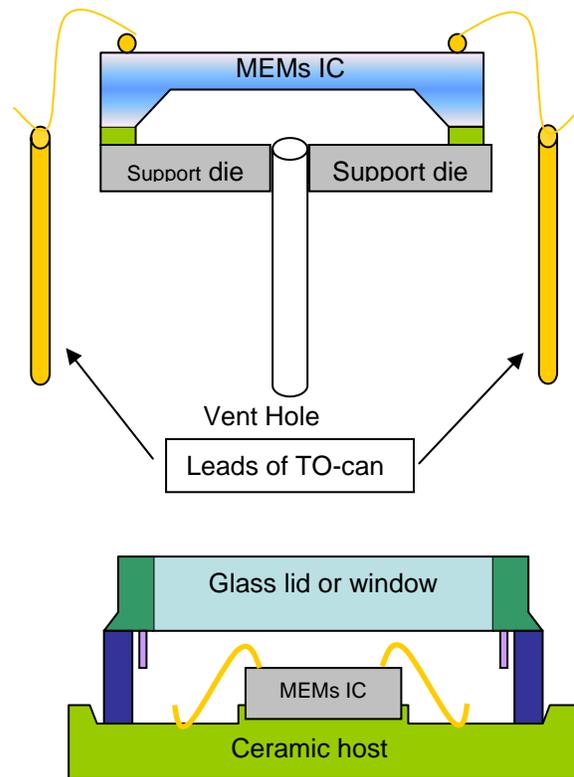
Figure 8A & 8B. Schematic of MEMs pressure sensor, and MEMs fiber optic mirror-array, respectively speaking.

Screen Print Test Pattern
Figure 9 shows the test pattern we used, and the cured photo. The smallest row reveals a masked off region of 5 mil x 5 mil pads, spaced at 8 mil, with the largest row containing 12 mil x 12 mil pads at 18 mil pitch. The array was designed to be an hour-glass shape, so that we could monitor whether the direction of the squegee stroke influenced the shape of the masked-off pads. Most wire bonds pads are 4 mil x 4 mil, hence our decision to study whether or not I/Os could be masked off.
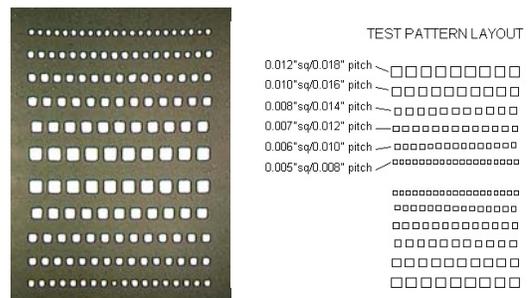
Figure 9. Test Pattern array and photo of dummy Si chip with screen print passivation coating.

We used a calendard 325 mesh containing 0.75 mil diameter stainless steel wire, with 0.5 mil emulsion. We recommend an amber-colored, polymer squeegee blade, which rolls nicely across the metal mesh. Print parameters need to be optimized for any screen print job, depending on print thickness, pitch, or shape of the masked off region, but we found the following parameters to work well: snap-off distance of 60-80 mils, stroke velocity of 1 -1.5 " per second; stroke force of 20 -30 lbs, squeegee angle 45 degree.

CONCLUSION
Screen printable polymers, acting like passivation, are certain to play a role in wafer level packaging. We have demonstrated that it can be used in several applications such as protection of bio-MEMs finger print sensors, memory device, and opto-electronic packaging. A test pattern was designed, in order to observe the smallest pattern or array that could be masked-off.

We also believe it advantageous as a buffer coating layer, in its cured form, on the top side of wafers, due to recent packaging trends like 3D or chip stacking. The "industry is working on new ultra-integration strategies, such as SiP or 3D chip staking, the latter achieved by wafer-to-wafer bonding, or die-to-wafer", says Peter Singer, editor-in-chief of Semiconductor International. [9] Our product is the ideal candidate for adhesive applications at the wafer level.

In order for 3D chip stacking to occur, wafer thinning technologies must be realized. Back-lapping, or wafer thinning, involves placing the wafer face down into wax and grinding the silicon off the back side until the desired thickness is achieved. This mechanical stress can tear off metallization lines, cause electrical shorts, or "dead" devices. It has been reported that when using top-side polyimide passivation coatings, wafer yields increased from 53.7% to 88% compared with un-coated devices, after probe card testing. [10] With ultra-integration, it is common for 2-, 3-, 4- or more stacked die in package, occupying the same dimensions as single-chip packages in the past. [10] Nearly 85% of DRAM memory devices are shipped as modules, with 3D stacking playing a vital role. [11]

In opto-devices, work at Georgia Tech is underway for chips that communicate with eachother by electrical and optical signals. [12] Certainly glass lids, or windows, will be used for protecting, sealing, and transmitting the light correctly, and wafer level sceen printing of adhesives and coatings will be needed.

REFERENCES

1. Reed, Greg, "Innovation Keys a Comeback", The Electronics Industry Yearbook, 2004 ed., p. 97
2. Estes, R. H., Pernice, R. F., and Hannafin, J. J., "Evaluation of Isotropically Conductive Adhesives for Solder Replacements". Proceedings of the ISHM Conference, Boston, MA., 1994, pp. 561-565.
3. Li, L., Morris, J.E., "Reliability and Failure Mechanisms of Isotropically Conductive Adhesive Joints", Proceedings of the IEEE Conference, 1995, pp. 114-120.
4. Breed, Steven., "Stencil Adhesive Deposition", Surface Mount Technology Magazine, January, 1998, pp. 68-73.
5. Lin, J. K., Lytle, W., Scharr, T., Subrahmanyan, R., Sharma, R., "Conductive Polymer Bump Interconnects", Proceedings of the ECTC Conference, Orlando, FL, 1996, pp. 1059 – 1068.
6. ShellCase, Ltd. Israel, web site info.
7. Cupers, D., Van Doorelaer, G., Van Den Steen, J., "Assembly of an XGA 0.9" LcoS Display using Inorganic Alignment Layers for VAN LC", Proceedings of the European Socitety of Information Display Conference, Paris, 2003, pp. unknown
8. Gilleo, K., "MEMs Packaging Issues and Materials", Journal of Advancing Microelectronics, 2000, Vol.27, 6, pp. 9-13.
9. Singer, Peter, "A New Era", The Electronics Industry Yearbook, 2004, ed., p. 83
10. Kulesza, F. W., Estes, R.H., Spanjer, K., "A Screen Printable Polyimide Coating for Silicon Wafers", Solid State Technology Magazine, Jan., 1988, pp. unknown
11. Levine, Bernard, "Packaging Foundries at the Cutting Edge", Semiconductor Manufacturing Magazine, Sep., 2004, p. 37.
12. Singer, Peter, "A New Era", The Electronics Industry Yearbook, 2004, ed., p. 83