Conductive Adhesives for Thermal Management; Case Study Issues in Hybrid Microelectronics and Plastic IC Packaging

Michael J. Hodgin
Applications Engineering Manager
Epoxy Technology, Inc., 14 Fortune Drive, Billerica, MA. 01821
Phone 978-667-3805, Fax 978-663-9782, www.epotek.com

Abstract

This paper discusses silver filled and boron nitride filled epoxies for heat-sinking and thermal transfer. Case studies of thermal resistance calculations have been presented with comparisons made against eutectic die-attach.

Introduction

Specifically, the hybrid packages fit the TO format (transistor outline packages). TO packages TO-3, TO-5, TO-18, and TO-220 have been examined. The TO-220 case study dealt with a transfer molded plastic IC package (instead of metal cans) which used non-electrically conductive epoxy; while the other case studies dealt with silver filled epoxy used inside the hybrid TO cans. [1,2,3]

Experimental Discussion

Case study #1 demonstrated the thermal resistance of silver epoxy versus solder for 20 mil x 20 mil chips attached to the TO-18. The thermal resistance of junction-to-case (θJc) was determined. By knowing the chip dimensional area and the bond-line thickness (BLT), the thermal resistance results have been back calculated into bulk thermal conductivity values. Specifically, the eutectic die-attach demonstrated about 2°C cooler improvement over the epoxy die-attached chip. The soldered chip had a measured thermal resistance between 4.8 – 5.3°C / W, while the epoxied chip was 6.7 – 7.0°C / W. Using back-calculations, the BULK thermal conductivity of the solder was found to be about 41 W / m°K, while the epoxied chip demonstrated about 29 W / m°K.

The effect of BLT and chip area on thermal resistance measurements has also been demonstrated. The chip size varied from (20 mil x 20 mil) up to (120 mil x 140 mil). The results show that the larger the chip, the smaller the thermal resistance, which was expected. The effect on BLT was demonstrated from 0.5 mils to 5 mils, and the results suggested that the lowest thermal resistance has been obtained on the smallest BLT, which was also expected.

Case Study #2 is similar to Case Study #1, however it used the TO-5 package. In this case, the size of the chip is 75 mil x 80 mil with a 0.5 mil BLT. Similar to Case Study #1, the thermal resistance junction-to-case (θ Jc) has been measured. Again, the thermal resistance of the soldered chip was about 2°C cooler improvement over the epoxied chip. θJc for the soldered chip was 9.0 – 10.3°C / W, while the epoxied chip was 11.3 – 12.6°C / W. Having back-calculated the BULK thermal conductivity, this study suggested that solder had about 0.36 W/m°K while the epoxy demonstrated 0.27 W/m°K.

Reprinted with permission from the Proceedings of the Technical Program, 28th Annual New England IMAPS Conference, Boxborough, MA., May 8, 2001.

Case Study #3, is similar to Case Study #2, but it used a TO-3 package. The θJc was determined for 7 silver filled commercially available epoxies and compared to soft solder controls. The die were bipolar transistors from Motorola; 2N-3055 chips which were 120 mil x 140 mil. A minimum of five samples were tested for each epoxy. The average BLT was calculated for each epoxy. The θJc for solder controls was 0.90°C / W. The best epoxy tested showed a θJc of 0.99°C / W, while the worst epoxy showed 4.9°C /W. [1]

Having back-calculated the BULK thermal conductivity, the solder control was found to be 2.56 W / m°K, and the best epoxy value was 1.14 W / m°K. The worst epoxy tested was found to be 0.35 W / m°K. The results of this study are somewhat contradictory to Case Study #1. It can be concluded that the package design of Case Study #1 was much better constructed than this example. The former resulted with solder having a BULK thermal conductivity of 41 W / m°K, while the latter had 2.56 W / m°K. Comparing the epoxy attached chip in Case Study #1 and #3, the former had 29 W / m°K, while the latter had 1.14 W / m°K.

Case study #4 is similar to #3 above in that it used the same TO-3 package and the same chips, however, this study monitored the thermal resistance as a function of 150°C / 1000 hr. burn-in, as well as varied the effect of BLT . Six commercially available silver-filled epoxies were tested against soft-solder controls. θJc observations were made by using IR Thermograph; the model was Agema Thermovision 782. A color coded temperature gradient, accurate to 0.1°C, was produced and recorded on the thermogram. [3]

θJc measurements were the lowest for the solder chip, which was expected, and a resultant value of 0.3°C / W. The highest θJc obtained was 1.45°C / W for an epoxied chip. Back-calculating for BULK thermal conductivity suggested that the solder was 15.6 W / m°K, and the worst epoxy was 3.2 W / m°K. This study also monitored the thermal resistance as a function of storage temperature for 150°C / 1000 hr. duration. With the exception of solder, the data suggested that thermal resistance always increases during burn-in of the epoxy in packages. It is proposed that burn-in causes the epoxy to outgass hydrocarbon materials, which will contribute to pin-holes and voiding in the bond-line therefore impeding thermal transfer. Lastly, the study monitored the effect of BLT on thermal resistance. All six epoxy samples were attached to the TO headers with controlled BLT of 2 mil, 3 mil, and 4 mil. The solder controls were not included in this matrix because they were purchased commercially and were not prepared in the laboratory. The results suggested that the lowest thermal resistance was obtained from the 2 mil BLT, expectedly. All epoxies tested demonstrated this condition. As example, Adhesive A had 0.33°C / W for 2 mil BLT, 0.36°C / W for 3 mil BLT, and 0.41°C / W for 4 mil BLT. Presumably, a thinner BLT provides a more direct path for heat transfer. Unfortunately, two of the six epoxies tested had such high thermal resistance under 3 and 4 mil BLT condition, that they were immeasurable.

Case Study #5 differed in a few ways from the examples above. First of all, it used electrically non-conductive epoxy instead of silver-filled. Four commercially available boron-nitride filled epoxies were obtained for the study. Second, unlike the above cases, the study used epoxy outside of the package. A TO-220AC package with Al tab was glued to copper heat sink outside the package. Thermal resistance from the package was determined for each epoxy, and compared with the expected thermal resistance obtained from the vendor's data sheets. [4]

The TO-220AC package glued to the heat sink had a surface area of 100 mm-sq. The BLT was fixed at 3 mils for all epoxies tested. The lowest θJc obtained was 0.6°C / W, while the worst epoxy had 1.2°C / W. Having back-calculated for BULK thermal conductivity, the study suggested the best boron nitride filled epoxy was capable of 1.25 W / m°K, while the worst epoxy was 0.62 W / m°K. The strength of the bond between package and heat sink was determined initially; and then as a function of 1000 Thermal Cycles (-55°C to 125°C) and 360 hours of Damp Heat (85°C / 85% RH). The results of the study suggested that the best thermally conductive epoxy lowest thermal resistance) was not the most superior product during environmental testing. Rather, of the four epoxies tested for thermal resistance, the product ranked #2 in the study for heat transfer out-performed all others during environmental screening. The results of the thermal and environmental tests were necessary in determining which product would be selected for mounting a heat-sink on top of a microprocessor chip.

Summary of Results

Case Study	Package Format	Product ID	Die Size or square Area of heat path	Bond-Line Thickness (BLT) or length of heat path (units in mils)	Thermal Resistance θJc (°C / W)	Back-calculated Thermal Conductivity (W / m°K)
#1	TO-18	solder	20 mil x 20 mil	2	4.8 - 5.3	41
	TO-18	Ag epoxy	20 mil x 20 mil	2	6.7 - 7.0	29
#2	TO-5	solder	75 mil x 80 mil	0.5	9.0 - 10.3	0.36
	TO-5	Ag epoxy	75 mil x 80 mil	0.5	11.3 - 12.6	0.27
#3	TO-3	A	120 mil x 140 mil	0.37	1.52	0.56
	TO-3	B	120 mil x 140 mil	0.37	2.43	0.35
	TO-3	C	120 mil x 140 mil	0.34	0.99	0.81
	TO-3	D	120 mil x 140 mil	0.45	2.7	0.38
	TO-3	E	120 mil x 140 mil	0.68	1.37	1.14
	TO-3	F	120 mil x 140 mil	0.25	1.52	0.38
	TO-3	G	120 mil x 140 mil	1.4	4.9	0.66
	TO-3	solder	120 mil x 140 mil	1	0.9	2.56
#4	TO-3	A	120 mil x 140 mil	2	0.33	14.2
	TO-3	B	120 mil x 140 mil	2	0.31	15.1
	TO-3	C	120 mil x 140 mil	2	0.4	11.7
	TO-3	D	120 mil x 140 mil	2	0.5	9.4
	TO-3	E	120 mil x 140 mil	2	1.45	3.2
	TO-3	F	120 mil x 140 mil	2	1.38	3.4
	TO-3	solder	120 mil x 140 mil	2	0.3	15.6
#5	TO-220AC	A	100 mm-sq	3	0.7 - 1.0	1.07
	TO-220AC	B	100 mm-sq	3	0.6 - 0.9	1.25
	TO-220AC	C	100 mm-sq	3	0.8 - 1.0	0.94
	TO-220AC	D	100 mm-sq	3	1.2 - 1.6	0.62

Conclusions

- The package format and design make a big difference in thermal resistance and back-calculated BULK thermal conductivity (Case study # 3 versus #4).
- Solder attachment of chips is always more cool (better thermal management) than epoxy attached ICs (all cases).
- Epoxy attached chips are about 2 degrees more hot than soldered chips (Case study #1 and #2).
- Thermal conductivity of silver epoxy can nearly be equal to that of solder (Case study #4 and Case study #3) by comparing the respective thermal resistance from package.
- The thinner the bond-line thickness (BLT), the lower the thermal resistance (Case study #1 and #4) and the better BULK thermal conductivity.
- Boron Nitride filled epoxy demonstrated BULK thermal conductivity values similar with silver epoxy in other packages (Case study #5) and can be an effective means of thermal management.

Acknowledgements

I would like to thank Phil Creter for inviting me into the session and his patience with extending the deadline for me. I would like to thank Dmitrius Hatgis of M/A-COM, and Jim Arangeo of Raytheon Company for helpful discussions about thermal resistance and thermal conductivity. I would also like to thank Gerard Litjen of Philips CFT in The Netherlands for experimental work with the BN filled epoxies. Also, special thanks to Brenda Kearney for proof-reading, editing, and grammatical comments during the generation of the rough drafts. Lastly, this paper would not have been possible without the support of the entire Technical Services Group at EPOTEK. I thank them for their support of my projects over the years.

References

1. C. Mitchell and H. Berg, Use of Conductive Epoxy for Die Attach, *International Microelectronics Symposium* (1974), pp. 52 – 58.
2. R. H. Estes, F. W. Kulesza, and C. E. Banfield, Recent Advances Made in Die-Attach Adhesives for Microelectronic Applications, *Proceedings of the International Symposium of Hybrid Microelectronics* (1985), Anaheim, CA, pp. 391 - 401.
3. R. H. Estes and R. F. Pernice, Die Attach Adhesives Evaluation of VceSAT and θJc Performance in Power Devices, *Proceedings of the International Symposium on Microelectronics* (1989), Baltimore, MD, pp. 664 – 669.
4. M. J. Hodgin and R. H. Estes, Advanced Boron Nitride Epoxy Formulations Excel in Thermal Management Applications, *Proceedings of the NEPCON WEST Technical Program* (1999), Anaheim, CA, pp. 359 – 366.