# Study of RF Flip-chip Assembly with Underfill Epoxy

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**Abstract**

*Flip-chip assembly technology is becoming more and more important to radio frequency (RF) MCM with the following advantages: automated assembly, compact size, low cost, low cross talk, and low insertion loss. However, flip-chip assembly also demands careful evaluation of solder joint reliability. For an assembly with a large MMIC chip or with a polymer substrate, underfill epoxy should be used to enhance the solder joint reliability. For a GaAs-on-Duroid flip-chip assembly with a chip size of 1.380mm x 4.700mm the fatigue lives could be increased from 1,300 to 11,000 cycles by the use of epoxy. Epoxy enhances solder reliability; however, it may affect the electrical performance. Experimental studies have been conducted to measure the additional insertion loss resulting from the underfill epoxy. The additional loss is less than 1dB, and it is acceptable to many RF applications.*

## 1. Introduction

Flip-chip assembly of microwave/millimeter-wave devices offers many advantages over conventional packaging approaches such as low inductance, capacitance and resistance [1]. The improved interconnect performance, high reliability, and low cost are the motivation to applying flip-chip assembly to MMIC [2]. In addition, this assembly technology led to reduced losses of feed lines because of its low insertion loss and flexibility of mounting the MMIC directly on the back structure of the planar patch antenna [3]. In general, flip-chip assembly of RF MCMs has the following advantages: automated assembly, compact size, low cost, low cross talk, and low insertion loss.

So far, most of RF flip-chip assemblies are GaAs-on-ceramics with good coefficient of thermal expansion (CTE) matches. However, with the advancement of device and substrate technologies, large size GaAs chips and/or polymer substrates may be assembled for high-performance, low-cost applications. As a result, solder joint reliability could become a major concern, and it may demand the use of underfill epoxy to enhance the reliability. Epoxy underfilling the gap between the GaAs chip and the polymer substrate can significantly reduce the CTE mismatch and result in an acceptable fatigue life. It is commonly used for low-cost microelectronic flip-chip assemblies; however, it may cause potential RF performance degradation.

In order to understand the problem quantitatively, a solder joint reliability model has been established to characterize the reliability enhanced by the underfill epoxy. Two GaAs chips studied had dimensions of 1.106mm x 1.380mm x 0.635mm (chip #1) and 4.700mm x 1.380mm x 0.635mm (chip #2) [4]. Their assemblies on a ceramics or a Duroid substrate were modeled with or without underfill epoxy. In addition, RF performance of GaAs-on-ceramics assemblies has been measured to understand the effect of the underfill epoxy.

## 2. Reliability Modeling

Three models have been developed for the reliability analysis, which are 1) solder joint profile prediction, 2) finite element analysis (FEA), and 3) fatigue life estimation. The solder joint profile was obtained by using Surface Evolver, and the detail of this model can be found in [5]. The last two models are to be described below.

Figure 1 shows the mesh of the finite element model of the assembly with underfill epoxy. Because of symmetry, only 1/4 of the assembly was modeled. Typically, the finite element deformation/strain/ stress analysis for flip-chip or BGA assemblies uses global and local models [5]. In this case, since the joint number is only six, it is possible to merge the global model and local model into one for computational efficiency. In this model, the 20-node quadratic brick

element and 15-node quadratic triangular prism element were used for thermal induced strain/stress/fatigue analysis. There are four layers of elements in the solder joint. The model was established using Patran 3, and the computation used Abaqus 5.6. The material properties (CTE and Young's modulus) are listed in Table 1. The plastic properties of solder joint were taken from [5]. The results obtained from the model were strain/stress distributions and the maximum inelastic strain energy density in the solder joint. The maximum inelastic strain energy density was used to estimate the fatigue life of solder joint.

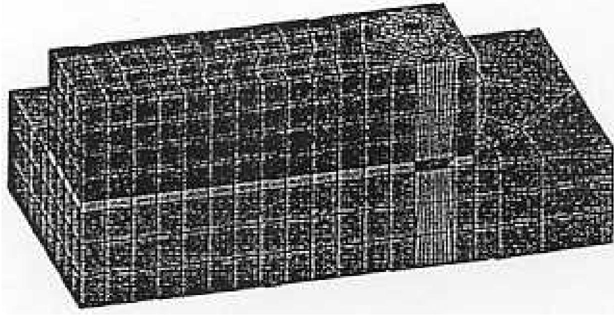

**Figure 1. The mesh of the finite element modeling.**

**Table 1: The mechanical properties for FEM simulation.**

| Properties | CTE ($10^{-6}$ /K) | Modulus (Mpa) | Tg (°C) |
|---|---|---|---|
| GaAs | 5.7 | 112815 | |
| Epoxy(U300) | 105 | 7500 | 130 |
| Duroid | 17 | 2070 | |
| Ceramic($Al_2O_3$) | 5.6 | 372384 | |

In the fatigue estimation, the inelastic strain energy density method was chosen for the fatigue calculation because extensive experimental data had been used to derive the correlation formula [6]. The cyclic inelastic strain energy density (ΔW) calculated by FEA was the failure indicator. ΔW was correlated with cycles for crack initiation and propagation. Since the elastic strain energy was recoverable, only plastic and creep strain energy densities were used in the estimation. The accumulated inelastic strain energy reached a stable level after the second cycle, so the local model calculated only two thermal cycles. The maximum energy density of the second cycle was used for estimation. The inelastic strain energy density was defined as

$$\Delta W = \int_C \tau_{ij} d\varepsilon_{ij}^P + \int_C \tau_{ij} \dot{\varepsilon}_{ij}^C dt \qquad (1)$$

where $\tau_{ij}$ are the stress components, $d\varepsilon_{ij}^P$ are the incremental plastic strain components, and $\dot{\varepsilon}_{ij}^C$ are the creep strain rate components. The empirical relations developed by Daveaux [6] for near eutectic Sn-Pb solders were:

$$N_0 = 7860 \Delta W^{-1.0} \qquad (2)$$

$$da/dN = 4.96 \times 10^{-8} \Delta W^{1.13} \qquad (3)$$

where $N_0$ is the number of cycles before a crack forms, and $da/dN$ was the area crack growth rate. The unit for $\Delta W$ was psi. The numbers of cycles of the solder fatigue was estimated as

$$N_f = N_0 + a/(da/dN) \qquad (4)$$

Where $a$ is crack length of the solder joint in inch and was chosen as 1.5 times the pad diameter.

In the present study, the solder pad diameter was 150μm, and the solder height was 70μm. The die thickness is 635μm, and the substrate thickness is 635μm. Eight cases were selected (see Table 2) to study the effects of die size, substrate material, and underfill epoxy on the fatigue life of solder joints. The fatigue analysis was based on the thermal cycling which temperature changes from 0 to 100°C with 240 seconds dwell and 150 seconds ramp. Figure 2 shows the plastic equivalent strain distribution of the solder joint at the corner of die. It can be seen that the maximum plastic equivalent strain is at the upper-right corner of the solder joint, and this is consistent with the experimental observation that cracks always happen here first for a convex shape joint.

**Table 2. The eight cases studied**

| Case | Dies | Material of substrate | With/without underfill epoxy |
|---|---|---|---|
| 1 | Chip #1 | Ceramic | Without |
| 2 | Chip #2 | Ceramic | Without |
| 3 | Chip #1 | Duroid | Without |
| 4 | Chip #2 | Duroid | Without |
| 5 | Chip #1 | Ceramic | With |
| 6 | Chip #2 | Ceramic | With |
| 7 | Chip #1 | Duroid | With |
| 8 | Chip #2 | Duroid | With |

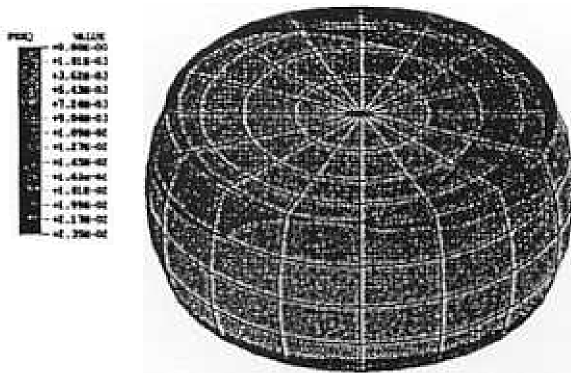

**Figure 2. The distribution of equivalent plastic strain in the solder joint.**

Figure 3 shows the fatigue life of the eight cases listed in Table 2. Without underfill epoxy, the fatigue life of the assembly with Duroid substrate and die size of 4.700mm × 1.389mm (chip #2) is only 1,300 cycles. The fatigue life of the assembly with a different ceramic substrate is 3,300 cycles. The Duroid substrate decreases the fatigue life greatly. The Duroid substrate leads to a larger global mismatch on solder joint due to its larger CTE (17ppm) compared with that of ceramic (5.6ppm). For the assembly with the Duroid substrate and without underfill epoxy, the fatigue life is too small to be acceptable. In order to increase the reliability of the assembly, underfill epoxy was chosen to increase the fatigue life. As shown in Figure 3, the underfill epoxy increases the fatigue life of the assembly with chip #2 and with duroid substrate from 1,300 to 11,000 cycles.. The underfill epoxy reduced the global mismatch of solder joints and resulted in a longer fatigue life of solder joints. The effect of underfill epoxy is very impressive . However, the underfill epoxy may affect electrical performance and this effect is to be discussed next.

## 3. RF performance measurement

Two GaAs chips containing coplanar-waveguide (CPW) sections were selected for experiment. The chip dimensions were 1.106mm × 1.380mm × 0.635mm (chip #1) and 4.700mm × 1.380mm × 0.635mm (chip #2), respectively [4].The 50Ω CPW through-lines on the chips had two different lengths of 0.600mm and 4.125mm. Six silver bumps on the edges of each chip were located at the end of CPW through-line and ground plane for interconnection. The bump dimension is 75μm in height and 150μm in diameter. The ceramic substrate ( 25.4mm x 25.4mm x 0.508mm ) had a sputtered thin-film of TiW (0.02μm) with 5μm Au for circuits. 50Ω CPW transmission line and multi-line-TRL calibration set were fabricated on the ceramic substrate for RF measurement.

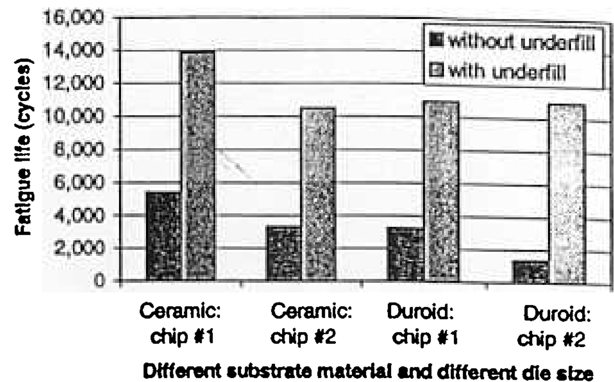


**Figure 3: fatigure life of defferent assemblies.**

The chip was bonded on the substrate by a thermosonic flip-chip bonding technology [7,8]. The bonding parameters were: 8.5 watts ultrasonic power at 180 °C for 500 ms, with 1.575kg bonding force. For the assembly with underfill epoxy, the epoxy (U300 from Epoxy Tech. Inc., with $\varepsilon_r$=4.1 and tanδ=0.009 at 100 KHz) filled the gap between the chip and the substrate and cured at 120 °C for 25 minutes. RF measurements were performed on a HP8510 network analyzer with on-wafer probes for a frequency range extending to 40 GHz. Measurements on assemblies for chip #1 and chip #2 were carried out before and after filling the epoxy.

Figures 4 and 5 show measured S-parameters of the flip-chip assembly for chip #1 with and without underfill as a function of frequency and Figures 6 and 7 show the same measurements for the assembly with chip #2. Comparing the measured results of the two flip-chip assemblies with and without underfill, we see two kinds of effects due to underfill: the return loss and insertion loss of flip-chip assemblies increase and the frequencies of minimum reflection shift downwards. However, the additional loss due to underfill epoxy is small as shown in Figures 8 and 9. In fact, the additional loss is less than 0.6 dB for the flip-chip assembly with chip #1 and less than 1 dB for the flip chip assembly with chip #2 at 40 GHz. The frequency shifts can be predicted accurately [9]. As a result, for most of RF applications, the effects of the underfill epoxy could be acceptable.

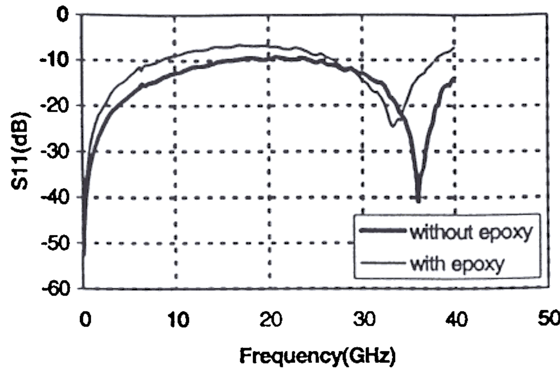


**Figure 4. Comparison of measured $S_{11}$ of flip-chip assembly with and without underfill for chip #1.**

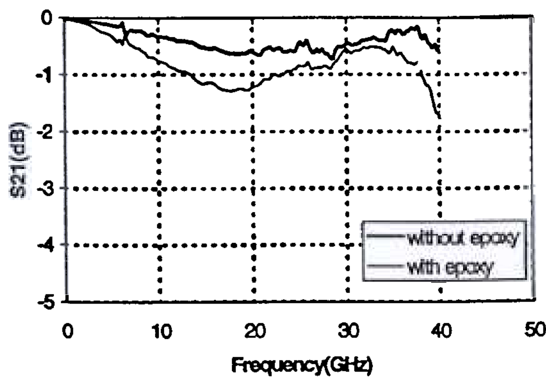


**Figure 5. Comparison of measured $S_{21}$ of flip-chip assembly with and without underfill for chip #1.**

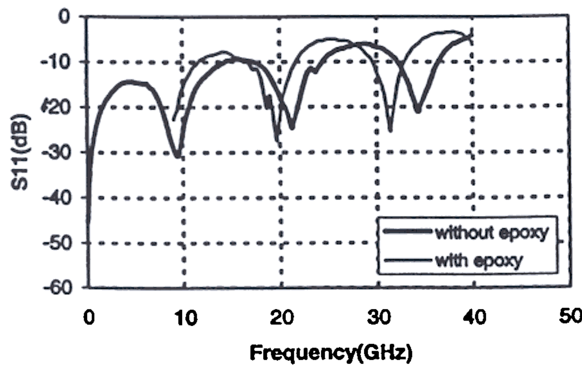


**Figure 6. Comparison of measured $S_{11}$ of flip-chip assembly with and without underfill for chip #2.**

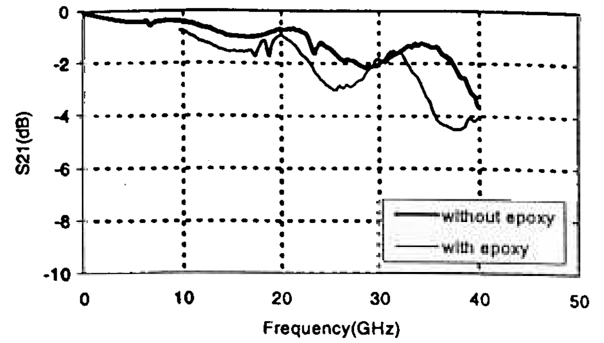


**Figure 7. Comparison of measured $S_{21}$ of flip-chip assembly with and without underfill for chip #2.**

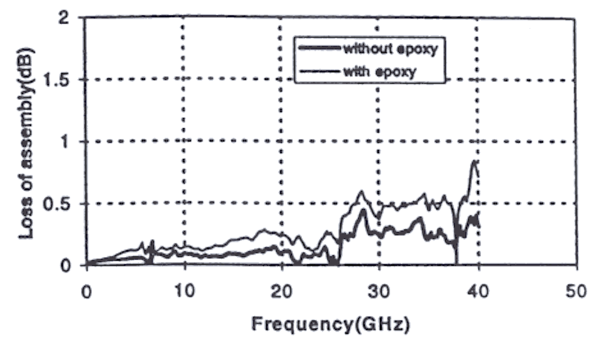


**Figure 8. Comparison of calculated loss of flip-chip assembly with and without underfill for chip #1.**

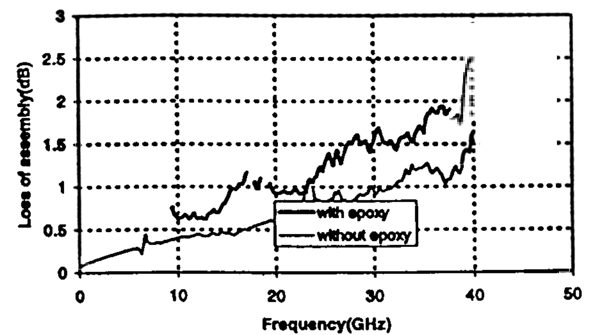


**Figure 9. Comparison of calculated loss of flip-chip assembly with and without underfill for chip #2.**

## 4. Summary

Underfill epoxy will assure reliable solder connections for RF flip-chip assemblies with large MMIC chips and/or polymer substrates. A solder joint reliability model has been established, and the

model confirmed the outstanding reliability enhancement by the epoxy. For a GaAs-on-Duroid flip-chip assembly with a chip size of 1.380mm x 4.700mm the fatigue lives could be increased from 1,300 cycles in the case without the epoxy to 11,000 cycles in the case with the epoxy. RF measurements have been conducted to characterize performance degradation. The additional loss was less than 1dB, and such a loss may be acceptable to many RF applications.

## 5. Acknowledgement

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